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OLMC configuration

16V8: I/O overview for Simple, Complex & Registered mode

Pin	Simple 16V8	Simple 16V8A	Complex	Registered
1	<Input	<Input	<Input	<Register Clock
19	<>I/O w/o FB	<>I/O	>Tri-Output w/o FB	«»Tri-I/O or Register
18	<>I/O w/o FB	<>I/O	«»Tri-I/O	«»Tri-I/O or Register
17	<>I/O w/o FB	<>I/O	«»Tri-I/O	«»Tri-I/O or Register
16	>Output w/o FB	>Output w/o FB	«»Tri-I/O	«»Tri-I/O or Register
15	>Output w/o FB	>Output w/o FB	«»Tri-I/O	«»Tri-I/O or Register
14	<>I/O w/o FB	<>I/O	«»Tri-I/O	«»Tri-I/O or Register
13	<>I/O w/o FB	<>I/O	«»Tri-I/O	«»Tri-I/O or Register
12	<>I/O w/o FB	<>I/O	>Tri-Output w/o FB	«»Tri-I/O or Register
11	<Input	<Input	<Input	<Register /OE

20V8: I/O overview for Simple, Complex & Registered mode

Pin	Simple 20V8	Simple 20V8A	Complex	Registered
1	<Input	<Input	<Input	<Register Clock
22	<>I/O w/o FB	<>I/O	>Tri-Output w/o FB	«»Tri-I/O or Register
21	<>I/O w/o FB	<>I/O	«»Tri-I/O	«»Tri-I/O or Register
20	<>I/O w/o FB	<>I/O	«»Tri-I/O	«»Tri-I/O or Register
19	>Output w/o FB	>Output w/o FB	«»Tri-I/O	«»Tri-I/O or Register
18	>Output w/o FB	>Output w/o FB	«»Tri-I/O	«»Tri-I/O or Register
17	<>I/O w/o FB	<>I/O	«»Tri-I/O	«»Tri-I/O or Register
16	<>I/O w/o FB	<>I/O	«»Tri-I/O	«»Tri-I/O or Register
15	<>I/O w/o FB	<>I/O	>Tri-Output w/o FB	«»Tri-I/O or Register
13	<Input	<Input	<Input	<Register /OE

‘<’ pin is input only
‘>’ pin is output only
‘<>’ pin direction is input or output, according to ACW bits
‘«»’ Tri-I/O or Register, according to ACW bits
‘«»’ Tri-I/O: pin is input/disabled or output, according to OE Product Term
‘«»’ Register: pin is input/disabled or output, according to /OE pin signal

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GAL pinouts (device in Edit mode; V_{EDIT}>12V)

20/24 pin GAL & ATF

6001 6002	22V10 20XV10 20RA10	20V8	18V10	16V8	DIL 24	 *20*		DIL *20*	 24	16V8	18V10	20V8	22V10 20XV10 20RA10	6001 6002
VIL	VIL	VIL			**1**				**24**			VCC	VCC	VCC
EDIT	EDIT	EDIT			**2**				**23**			VIL	VIL	P/V
VIL	P/V	RA1	VIL	VIL	**3**	***1***		***20***	**22**	VCC	VCC	P/V	VIL	VIL
RA0	RA0	RA2	EDIT	EDIT	**4**	***2***		***19***	**21**	P/V	P/V	RA0	VIL	VIL
RA1	RA1	RA3	RA3	RA1	**5**	***3***		***18***	**20**	RA0	RA0	VIL	VIL	VIL
RA2	RA2	VIL	RA4	RA2	**6**	***4***		***17***	**19**	VIL	RA1	VIL	VIL	VIL
RA3	RA3	VIL	RA5	RA3	**7**	***5***		***16***	**18**	VIL	RA2	VIL	VIL	VIL
RA4	RA4	RA4	SCLK	RA4	**8**	***6***		***15***	**17**	VIL	VIL	VIL	VIL	VIL
RA5	RA5	RA5	SDIN	RA5	**9**	***7***		***14***	**16**	VIL	VIL	VIL	VIL	VIL
SCLK	SCLK	SCLK	/STB	SCLK	**10**	***8***		***13***	**15**	VIL	VIL	SDOUT	VIL	VIL
SDIN	SDIN	SDIN	SDOUT	SDIN	**11**	***9***		***12***	**14**	SDOUT	VIL	VIL	SDOUT	SDOUT
GND	GND	GND	GND	GND	**12**	***10***		***11***	**13**	/STB	VIL	/STB	/STB	/STB

28 pin GAL

26CV12* 26V12C*				
	DIL 28		DIL 28	
	PIN		PIN	
VIL	1		28	VIL
EDIT	2		27	VIL
P/V	3		26	VIL
RA0	4		25	VIL
RA1	5		24	VIL
RA2	6		23	VIL
VCC	7		22	VIL
VIL	8		21	GND
RA3	9		20	VIL
RA4	10		19	VIL
RA5	11		18	VIL
SCLK	12		17	VIL
SDIN	13		16	VIL
/STB	14		15	SDOUT

* use 28 to 24 pin adapter with 22V10 target pinout

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Architecture Control Word

	Architecture Control Word (ACW)						
	MSB						LSB
82 BITS	81						0
	PT Disables	**XOR(n)**	**SYN**	**ACN1(n)**	**AC0**	**XOR(n)**	**PT Disables**
WIDTH	32	4	1	8	1	4	32
MAPPING	PTD63..PTD32	Pin12..Pin15	global	Pin12..Pin19	global	Pin16..Pin19	PTD31..PTD0
GAL16V8							
FUSES	#2191..#2160	#2055..#2052	#2192	#2127..#2120	#2193	#2051..#2048	#2159..#2128
GAL20V8							
FUSES	#2703..#2672	#2567..#2564	#2704	#2639..#2632	#2705	#2563..#2560	#2671..#2640

	Architecture Control Word (ACW)						
	MSB						LSB
82 BITS	81						0
	XOR(n)	**SYN**	**ACN1(n)**	**PT Disables**	**ACN1(n)**	**AC0**	**XOR(n)**
WIDTH	4	1	4	64	4	1	4
MAPPING	Pin12..Pin15	global	Pin12..Pin15	PTD63..PTD0	Pin16..Pin19	global	Pin16..Pin19
GAL16V8A							
FUSES	#2055..#2052	#2192	#2127..#2124	#2191..#2128	#2123..#2120	#2193	#2051..#2048
GAL20V8A							
FUSES	#2567..#2564	#2704	#2639..#2636	#2703..#2640	#2635..#2632	#2705	#2563..#2560

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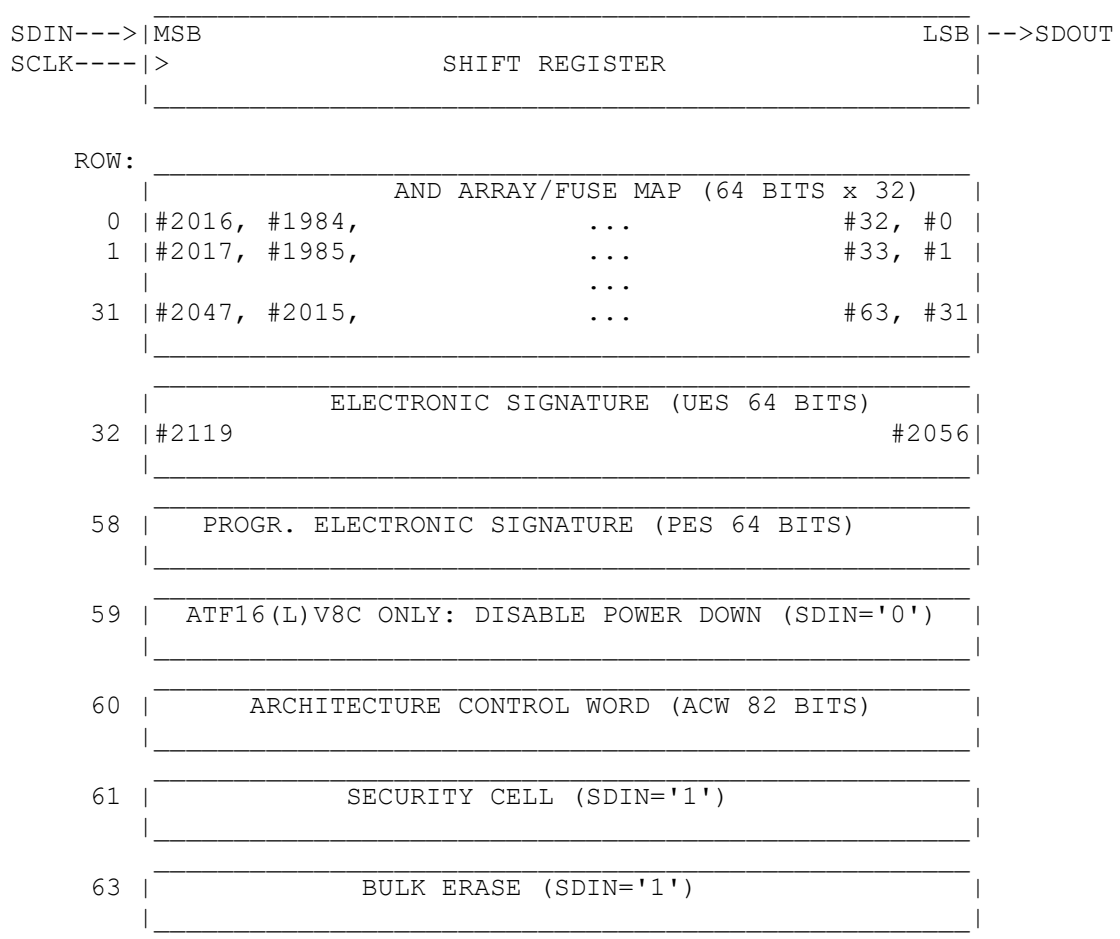
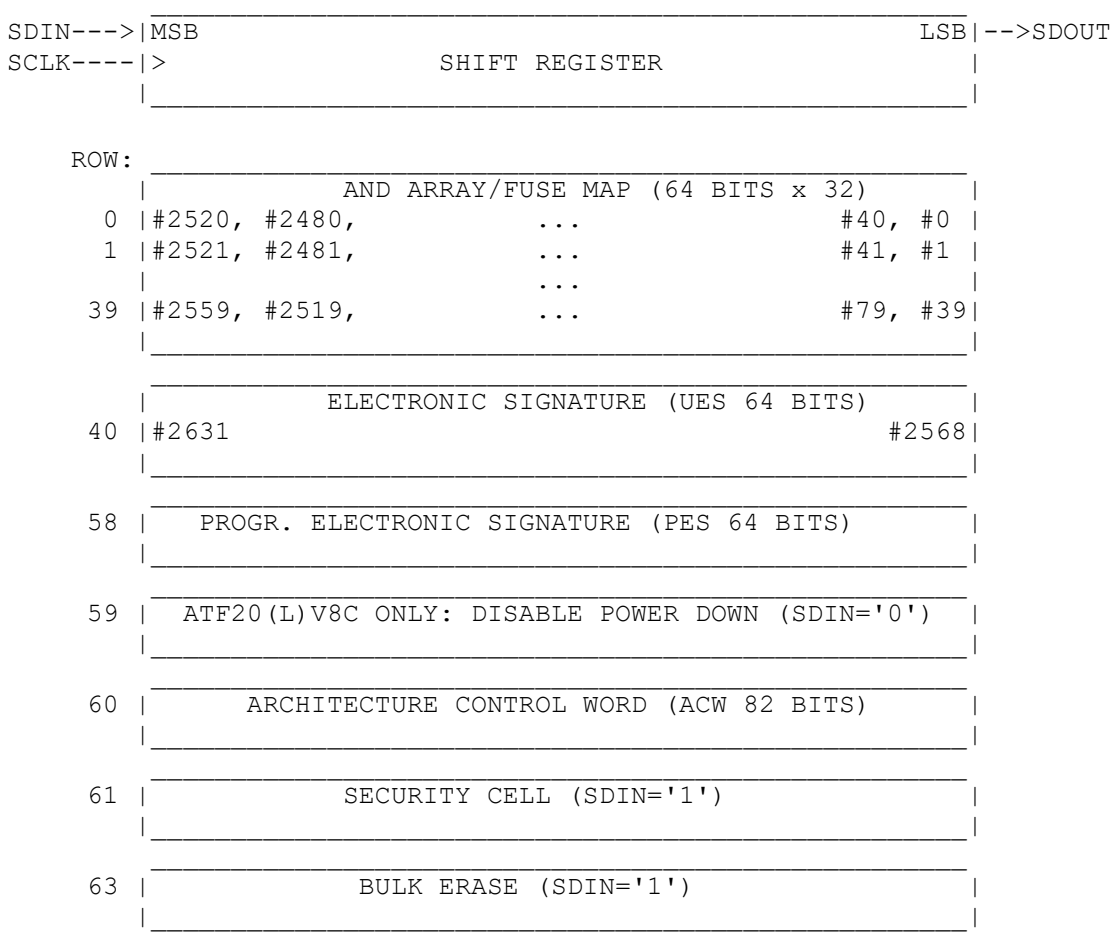
GAL16V8 Row Addresses Map Block Diagram



GAL_16V8_20V8_22V10_specific

GAL20V8 Row Addresses Map Block Diagram



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GAL22V10 Row Addresses Map Block Diagram